IN THE SPECIFICATION:

Please amend paragraph number **[0019]** as follows:

[0019] Emitter tip 13 is positioned on substrate 11 and conductive layer 12. Emitter tip 13 serves as a cathode conductor, and although any shape providing the necessary emitting properties can be used, a conical shape is preferred. Emitter tip 13 may comprise any emitting material, but preferably comprises a low work function ~~material - a~~ material, a material which requires little energy to emit the ~~electrons - such~~ electrons, such as silicon or molybdenum.

Please amend paragraph number **[0023]** as follows:

[0023] Insulating layer 20 is located between gate electrode 15 and focusing electrode 19, having an insulating ridge (e.g., a sidewall) extending closer to emitter tip 13 than either the gate electrode 15, the focusing electrode 19, or both. Insulating layer 20 serves to separate and insulate gate electrode 15 and focusing electrode 19 and the voltage differential between them. Any insulating material exhibiting such properties can be employed as insulating layer 20, such as dielectric materials like silicon nitride or silicon oxide. Preferably, insulating layer 20 comprises silicon oxide.

Please amend paragraph number **[0025]** as follows:

[0025] A FED containing the aperture-type focusing electrode of the present invention can be formed by many processes, including the process described below and illustrated in FIGS. 2-8. ~~A~~ Referring to FIG. 2, P-type silicon layer, preferably single crystal silicon, is used as a substrate to form the emitters. In this silicon layer a series of elongated parallel N-conductivity regions or wells are formed by a doping process, such as diffusion and/or ion implantation. The size and spacing of the wells can be adjusted to accommodate any number of field emission sites. If desired, the P-type and N-type conductivities can be reversed. The undoped portions of the silicon layer are then selectively removed, leaving doped wells in the general shape and size of the emitters. The surface of the silicon layer and the emitters are then oxidized to produce a layer of silicon oxide, and then etched to produce emitter tip 13. Any

suitable oxidation process may be employed in forming the silicon oxide and any suitable etching process may be used to etch the tip.

Please amend paragraph number **[0026]** as follows:

[0026] The emitters can also be formed by an alternative process. In the alternative process, the silicon ~~layer or~~ layer, or any other suitable material for the ~~emitters is~~ emitters, is provided. Then, a layer of silicon ~~oxide or~~ oxide, or other suitable masking material for the underlying ~~layer is~~ layer, is formed over the silicon layer. Portions of the silicon oxide layer are then removed, preferably by a photolithographic patterning and etching process, to leave an oxide etch mask overlying the emitter sites. The silicon layer is then anisotropically etched, removing portions of the silicon layer underlying the oxide etch mask as well as portions not underlying the etch mask and forming emitter tips 13. The oxide mask is then removed.

Please amend paragraph number **[0027]** as follows:

[0027] Next, as illustrated in FIG. 3, first insulating layer 14′ is deposited. This insulating layer is selectively etchable with respect to the conductive layer 15′, as explained below. Suitable selectively-etchable materials include silicon nitride, silicon oxide, and silicon oxynitride. Preferably, silicon oxide is employed as first insulating layer 14′. The thickness of first insulating layer 14′ will determine the spacing of gate electrode 15 to emitter tip 13, as well as the spacing of gate electrode 15 to conductive layer 12. Therefore, first insulating layer 14′ must be as thin as possible, since small gate electrode 15 to emitter tip 13 distances result in lower emitter drive voltages. Yet the thickness must be large enough to prevent the oxide breakdown which occurs if gate electrode 15 is not adequately separated from conductive layer 12. For example, the thickness may range from about 0.3 to about 0.5 microns, and is preferably about 0.35 microns. Preferably, as depicted in FIG. 3, first insulating layer 14′ is a conformal ~~layer the~~ layer, meaning that layer is deposited so it conforms to the shape of emitter tip 13.

Please amend paragraph number **[0034]** as follows:

[0034] As illustrated in FIG. 5, opening 25 is then formed in conductive layer 19′, thus defining focusing electrode 19. Opening 25 is located above emitter tip 13 so the resulting focusing electrode 19 can collimate electron beam 17. Any removal process which forms opening 25 without attacking or degrading exposed portions of second and third insulating layers 8′ and 20′ can be employed. Preferably, opening 25 is formed by a photopattern and etch process.

Please amend paragraph number **[0041]** as follows:

[0041] FIGS. 9-14 illustrate the present invention in a FED containing a concentric-type electrode structure. A concentric-type electrode structure differs from an aperture-type electrode structure in that the focusing electrode 29, rather than located above, is located to the sides of the gate electrode, as shown in FIG. 9. In the present invention, gate electrode 23 and focusing electrode 29 are separated by an insulating layer containing insulating ridge 33, i.e., an upper surface extending above the upper surface of either the gate or focusing electrode. Like the aperture-type focusing electrode, the concentric-type focusing electrode collimates electron beam 17 emitted from each emitter tip 13 and reduces the area where the beam impinges on the phosphor coated display screen 16, thus improving the image resolution. Insulating ridge 33 separates gate electrode 23 and focusing electrode 29 and insulates the voltage differential between them.

Please amend paragraph number **[0047]** as follows:

[0047] Variations of the above structure and method are possible. If desired, a dual-insulating ridge can be fabricated by forming successive insulating layers 29′ (FIG. 14) instead of a single ~~insulating layer~~ focusing electrode 29. Moreover, additional focusing electrodes 33′ (FIG. 14) could be formed by forming additional vias in conductive layer 15′. Further, while the gate electrode and focus structure described above are preferably made of the same material and therefore require a single conducting layer, it is possible, but not preferable, to

modify the process to obtain two separate conducting layers, one for the gate electrode and another for the focus electrode.